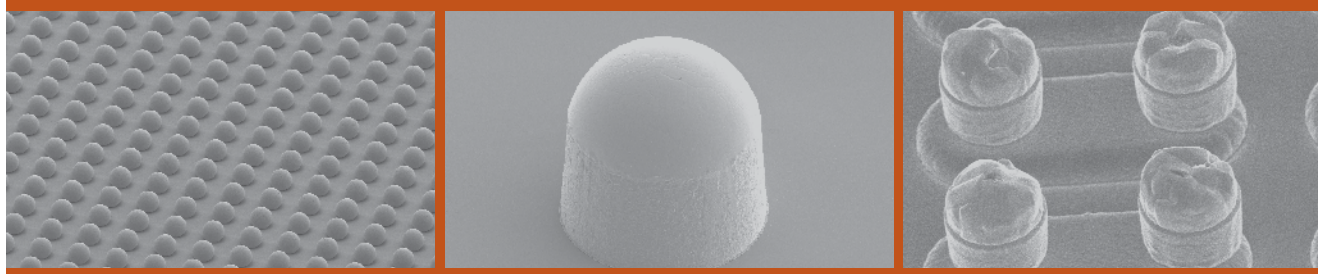


MICROSYSTEM INTEGRATION AND PACKAGING

Advanced Interconnect and Packaging Technologies



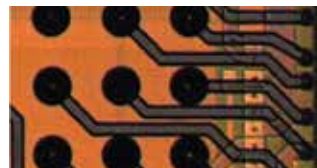
RTI International is home to one of the premier wafer bumping and wafer-level packaging research and fabrication facilities in the U.S. Our experts in material and electronic technologies have over 15 years of research, development, and implementation experience in all areas of bump interconnect technologies. From material characterization to prototype and proof of concept, to pilot-line and small-scale production, we tailor our capabilities to meet each client's unique requirements.

Solder Bumping and Wafer-Level Chip-Scale Packaging

RTI International is a world leader in advanced interconnect and packaging technologies. RTI provides access to state-of-the-art wafer bumping and wafer-level packaging (WLP) technologies, supporting small and mid-volume customers as well as developmental and prototyping applications. Services and processes we offer for advanced packaging and interconnect include:

- Bump on I/O pad
- Bump on polymer
- Polymer repassivation
- Single and multiple layer Cu redistribution
- Eutectic Sn/Pb, Pb-free, and Cu pillar bumping
- Design services.

Clients can take advantage of our standard repassivation, redistribution, and bumping processes and we can customize the processes; and materials used for your specific application. Multi-level metallization schemes employing inorganic or organic dielectrics are available. From design and fabrication of custom WLCSP and flip chip test vehicles to applying WLP processes on fully functional IC wafers, our flexibility and experience make RTI an ideal development partner.



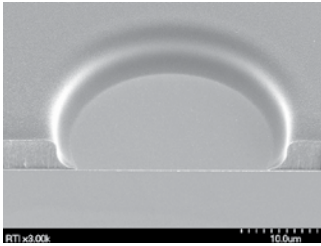
Repassivation and Cu redistribution with solder bumps



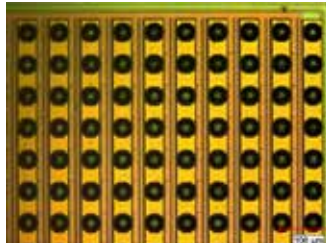
Two-layer Cu redistribution with two planar ILD layers

Electronic Material Characterization and Process Development

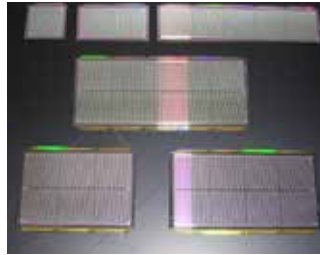
RTI's extensive experience in flip chip and wafer-level packaging makes RTI an ideal partner for suppliers developing new materials for advanced packaging, such as photoresists, polymer dielectrics, plating chemistries, and underfills. Our capabilities allow us to provide a full spectrum of services for evaluating new materials, from basic characterization and process parameterization to full implementation into WLP test structures, reliability testing, and analysis. We help you determine how your material performs in the fab environment and how it interacts with other processes and materials your customers use. We can also work collaboratively with you and your customers to develop new application-specific processes. As a not-for-profit company, RTI offers a unique development environment to its clients, providing access to world-class tools and technologies and allowing clients to generate information they need to better characterize and market their products.



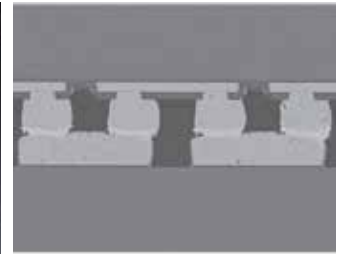
Evaluation and characterization of new electronic materials for advanced interconnect



25 μm diameter bumps on 50 μm pitch



Multi-chip particle detector modules with 50 μm I/O pitch



10 μm pitch Cu-Sn bump bonding

Ultra-Fine-Pitch Flip Chip Bumping

RTI is a world leader in ultra-fine-pitch flip chip technology, and our standard 50 μm I/O pitch process enables an interconnect density of 40,000 I/O per cm². Originally developed for advanced multichip module technologies in the 1990s, this technology has been used extensively in bumping pixilated particle detectors for high energy physics applications. Ideally suited for mating Si-to-Si devices, this process has also found applications in other advanced imaging, optoelectronic, and IC applications.

Flip Chip and Multi-Chip Module Assembly

RTI also offers flip chip assembly—from single chip placements to multichip module and system-in-package assembly of multiple die and components. Assembly is performed in a controlled environment for reduced particulate contamination. Our SET FC150 automated bonder provides the capability for flip chip and die bonding, thermocompression bonding, in situ reflow, and dispense of pre- and post-bond underfill materials with ±0.5 micron placement accuracy. RTI's patented plasma-assisted dry soldering (PADS) process is a revolutionary technology that allows soldering to be done without the use of flux. Recognized with an R&D 100 award, PADS has been successfully used in board-level soldering assembly as well as flip chip, optoelectronics, and MEMS applications.

Metal-Metal Bonding for 3D Integration

2.5D and 3D integration technologies are driving the integration of devices with extremely high interconnect densities for Si interposer and chip stacking applications.

RTI is a leader in the development and implementation of metal-metal bonding technologies, with proven technologies for fabricating and bonding CuSn-Cu and Cu-Cu full-area bump arrays with pitches as small as 10 microns. The resulting interconnect array is extremely strong mechanically and thermally stable at temperatures well above the thermal budget of most IC devices (>400°C). These interconnect structures can be applied to most IC wafers for high I/O density interconnection, chip stacking for 3D integration, Si-to-Si integration, and applications requiring thermal and mechanical stability at temperatures beyond that of typical solder materials.

Working with RTI

RTI is a not-for-profit company and ITAR-registered organization that offers a “safe harbor” development environment to our clients. We work with a diverse base of commercial clients, government agencies, and academic institutions, supporting our clients through application-driven technology development programs, custom prototyping, and small volume production. We also partner with external organizations for joint proposals in a variety of government and defense programs, including SBIR and STTR programs.

More Information

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